Amendments to the Drawings

The attached sheet of drawings include amendments to Fig. 6 and replaces the original sheet of drawings including Figs. 5 and 6. The amendments to Fig. 6 are for clarification purposes only and do not introduce new matter. It is respectfully requested that these amendments be accepted by the Examiner.

Attachment: Replacement Sheet for Figs. 5 and 6.

REMARKS

The present response cancels claims 5, 7 and 20 without prejudice or disclaimer as to the subject matter recited therein. In addition, claims 1, 4, 6, 14, and 18 have been amended. Accordingly, claims 1-4, 6, and 8-19 remain pending in the captioned case. Further examination and reconsideration of the presently claimed application are respectfully requested.

Allowable Subject Matter

Claims 10, 16, and 17 were deemed allowable if rewritten into independent form including all of the limitations of the base claim and any intervening claims. Applicants appreciate the Examiner's recognition of allowable subject matter. However, for reasons set forth below, it is believed that the independent claims and claims dependent therefrom are allowable in their present form over the art of record.

Objection to the Drawings

An objection was lodged against the drawings as failing to show every feature of the invention. In response thereto, Fig. 6 has been amended to contain an illustration of the biasing circuit having a transmission gate with p-channel and n-channel transistors configured with the claimed gate length and gate width specifications/ratios. Thus, the claimed inverter and second inverter is depicted in the detailed portion of Fig. 6 as each having a p-channel and a n-channel transistor. The gate widths (W) and the gate lengths (L1 and L2) are shown along with the ratios of the inverter relative to the second inverter (i.e., N:M = X:Y).

Applicants believe the amendments to Fig. 6 are fully supported by the originally-filed specification, including claims 2, 4, 8, and 10, for example. Accordingly, Applicants respectfully request removal of this objection.

Section 102 Rejection

Claims 1-9 and 18-20 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 4,906,871 to Iida (hereinafter "Iida"). The standard for "anticipation" is one of fairly strict identity. A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art of reference. *Verdegaal Bros. v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987); MPEP 2131. Furthermore, anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, as arranged in the claim. *W.L. Gore & Assocs. V. Garlock*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983). Using these standards, Applicants submit the cited art fails to disclose each and every element of the currently pending claims, some distinctive features of which are set forth in more detail below.

Iida does not teach or suggest a transmission gate having a gate terminal of a p-channel transistor coupled to a power supply voltage and a gate terminal of a n-channel transistor coupled to a ground supply voltage during power down of the circuit. Amended claim 1 indicates various voltages placed on the gate terminals of transistors which form the transmission gate during power down of the circuit. Specifically, the p-channel transistor gate terminal is coupled to a power supply voltage and the n-channel transistor gate is coupled to a ground supply voltage.

Contrary to claim 1, Iida specifically discloses the opposite to that which is claimed. For example, Iida denotes the p-channel transistor Q8 is coupled to a ground supply voltage, and the n-channel transistor Q7 is coupled to a power supply voltage (Iida -- Fig. 7). This is exactly the opposite of that presently claimed. In fact, the purpose of Iida is to render the transistors of the transmission gate conductive. No motivation is provided in Iida for reversing the conductive state of those transistors during power down or otherwise (Iida -- col. 4, lines 40-44). Thus, not only does Iida fail to disclose all that which is claimed, but specifically teaches the opposite of that which is claimed.

Iida does not teach or suggest removing the biasing and driving the biasing to a ground supply voltage during times when the differential signal is absent. Amended claim 18 makes clear that whenever a differential signal is absent, the input to the CMOS inverter is biased to a ground supply voltage. Specifically, Fig. 3 illustrates a CMOS inverter 36a/36e that is biased to a ground supply via transistor 40 (Specification -- Fig. 3). Nowhere is there any suggestion in Iida for biasing the input of inverter 20 to a ground supply during times when a differential signal is absent (Iida -- Fig. 3).

For at least the reasons stated above, Applicants believe independent claims 1 and 18, as well as claims dependent therefrom, are not anticipated by the cited art. Accordingly, removal of this rejection is respectfully requested.

Section 103 Rejection

Claims 11-15 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,518,789 to Grossmann (hereinafter "Grossman") in view of Iida. To establish a case of *prima facie* obviousness of a claimed invention, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. Second, there must be a reasonable expectation of success. As stated in MPEP 2143.01, the fact that references can be hypothetically combined or modified is not sufficient to establish a *prima facie* case of obviousness. *See In re Mills*, 916 F.2d. 680 (Fed. Cir. 1990). Finally, the prior art references must teach or suggest all the claim limitations. *In re Royka*, 490 F.2d. 981 (CCPA 1974); MPEP 2143.03. Specifically, "all words in a claim must be considered when judging the patentability of that claim against the prior art." *In re Wilson* 424 F.2d., 1382 (CCPA 1970). Using these standards, Applicants contend that the cited art fails to teach or suggest all features of the currently pending claims, some distinctive features of which are set forth in more detail below.

Iida and Grossman cannot be properly combined or, even if combined, do not teach or suggest a biasing circuit coupled to an input of each of the pair of inverters, or a pair of capacitors coupled between the pair of inverters and the respective pair of outputs of the differential amplifier. Present claim 11 describes a receiver that has a pair of inverters, a biasing circuit coupled to the inputs of each of the pair of inverters, and a pair of capacitors coupled between the pair of inverters and respective pair of outputs of the differential amplifier. Accordingly, claim 11 requires a double-ended output of the differential amplifier be biased using two inverters, two biasing circuits, and two capacitors arranged in the claimed fashion.

When combining Grossman and Iida, the Examiner correctly states that Grossman fails to teach a pair of inverters, a biasing circuit coupled to the input of each of the pair of inverters, and a pair of capacitors coupled between the pair of inverters and respective pair of outputs of the differential amplifier. However, the Examiner alleges that Iida teaches that which is missing from Grossman. Applicants respectfully disagree. Iida only teaches use of a single-ended output from resistor R3; thus, only a single

capacitor, a single inverter, and a single biasing circuit is shown, described, or suggested (Iida -- Fig. 3). In fact, Iida specifically teaches away from replicating the circuit and a double-ended output, since the purpose of Iida is to "provide a level shift circuit which requires a reduced number of circuit elements" compared to that of the prior art circuit of Fig. 1 which has a double-ended output, but absent a biasing circuit and capacitor at each output (Iida -- col. 1, lines 54-56, emphasis added; Figs. 1 and 3 in comparison). Moreover, Iida explicitly states that "it is noted here that the level shift circuit is made up of only capacitor 19, CMOS inverter 20, and the bias circuit or resistor R5" (Iida -- col. 4, lines 18-21, emphasis added). Iida continues by noting the level shifter of Fig. 3, when compared to that shown in Fig. 1, requires less number of circuit elements -- the primary goal of Iida (Iida -- col. 4, lines 22-25).

Accordingly, Applicants do not believe that Iida somehow implicitly suggests two inverters, two capacitors, and two biasing circuits, and simply omits to illustrate such items as suggested by the Examiner. Instead, Iida specifically requires only one of each item in an effort to reduce the number of circuit elements, and also to reduce the current dissipation in its level shifter apparatus. Therefore, one skilled in the art when looking to Iida would not be motivated to increase the circuit elements and the current dissipation by applying a double-ended output if only a single-ended output is suitable and necessitated by the teachings of Iida.

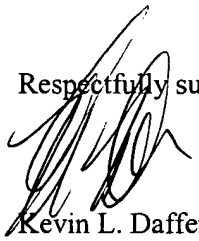
For at least the reasons stated above, Applicants believe independent claim 11 and claims dependent therefrom are patentably distinct over the cited art. Accordingly, removal of this rejection is respectfully requested.

CONCLUSION

The present amendment and response is believed to be a complete response to the issues raised in the Office Action mailed May 23, 2005. In view of the remarks herein traversing the rejections, Applicants assert that pending claims 1, 4, 6, 14, and 18 are in condition for allowance. If the Examiner has any questions, comments, or suggestions, the undersigned attorney earnestly requests a telephone conference.

No fees are required for filing this amendment; however, the Commissioner is authorized to charge any additional fees which may be required, or credit any overpayment, to Daffer McDaniel, LLP Deposit Account No. 50-3268/5298-13101.

Respectfully submitted,



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